REMARKS

Objection to Claim 4 under 37 CFR 1.83(a).

FIG. 1 shows the features of amended claim 4. According to claim 4, the first one of the plurality of wiring layers includes: a first wiring trace in the second wiring region disposed in the second direction; a second wiring trace in the second wiring region disposed in the second direction; and a third wiring trace in the first wiring region disposed in the first direction and electrically connecting the first wiring trace and the second wiring trace.

In FIG. 1, the first one of the plurality of wiring layers can be the M2 wiring layer electrically connecting diffusion regions of transistors (TR1, TR2, TR3, and TR4). The first one of the plurality of wiring layers includes a top trace (third wiring trace) running horizontally (first direction), a left trace (first wiring trace) on the left running vertically (second direction) over diffusion regions of transistors (TR1 and TR2) and a right trace (second wiring trace) on the right running vertically (second direction). The top trace (third wiring trace) electrically connects the left trace (first wiring trace) with the right trace (second wiring trace). The left trace (first wiring trace) and right trace (second wiring trace) are separated in the horizontal direction (first direction).

Because FIG. 1 shows all the features of claim 4, this ground for objection is respectfully traversed.

Objection to Claim 5 under 37 CFR 1.83(a).

As set forth in amended claim 5, the multi-layer wiring configuration includes a second one of the plurality of wiring layers. A memory array has bit lines formed with bit line wiring layers of the same material as the second one of the plurality of wiring layers.

New FIG. 7 has been added in the background of the invention, the figure presents no new matter as all items in the figure have been previously described in the specifications and claims as filed.

For example on page 2, lines 15-17 in the background of the invention in the specification as filed, describe a dynamic random access memory (DRAM) having capacitor over bit line (COB) memory cells in which a first wiring layer can also be used as a wiring layer for bit lines. This wiring layer can also be used as a first wiring layer for multi-layer wiring

configuration (page 3, line 1-2) as an interconnect for a peripheral circuit. See also page 17, lines 1-3 in the detailed description of the embodiments as well as originally filed claims 5, 6, 12, 19, and 20.

As is well known, information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter.[1]

For the reasons set forth above, this rejection is respectfully traversed.

Objection to Claim 6 under 37 CFR 1.83(a).

Claim 6 includes dynamic random access memory cells having a capacitor over bit line structure.

To address this, new FIG. 7 has been added in the background of the invention, the figure presents no new matter as all items in the figure have been previously described in the specifications and claims as filed. Arguments set forth in the rejection of claim 5 above are hereby incorporated.

For the reasons set forth above, this objection is respectfully traversed.

Objection to Claim 11 under 37 CFR 1.83(a).

Claim 11 includes a plurality of functional circuit blocks disposed in a matrix on the surface of a semiconductor substrate.

FIG. 3 includes a plurality of functional circuit blocks **100**. These functional circuit blocks **100** are disposed in a 1x3 matrix on the surface of a semiconductor device. Thus, it is believed that FIG. 3 illustrates this feature of claim 11.

For the reasons set forth above, this objection is respectfully traversed.

Objection to Claim 12 under 37 CFR 1.83(a).

As set forth in amended claim 12, the multi-layer wiring configuration includes a second one of the plurality of wiring layers. A memory array has bit lines formed with bit line wiring layers of the same material as the second one of the plurality of wiring layers.

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[1] See MPEP 2163.06

Arguments as set forth above in the rejection of claim 5 are hereby incorporated to overcome this objection.

Objection to the Specification:

The title amended to address this objection.

Other Corrections:

The paragraph beginning at Page 4, Line 22 has been replaced to correct a typographical error.

The paragraph beginning at Page 9, Line 4 has been replaced to correct a typographical error.

Rejection of Claim 4 Under 35 U.S.C. §112, First Paragraph.

The comments set forth for the objection to claim 4 are incorporated by reference herein.

Rejection of claims 1-13 Under 35 U.S.C. §112, Second Paragraph.

With respect to the rejection of claims 1 and 7, claims 1 and 7 have been amended to address this ground of rejection. The claims now refer to a "first one of a plurality of wiring layers" instead of a first wiring layer.

With respect to the rejection of claim 11, the comments set forth for the objection to claim 11 are incorporated by reference herein.

Rejection of Claims 1, 2, 7, 8 and 13 Under 35 U.S.C. §102(e) based on *Hiraga* (USP 6,064,097).

The rejection of Claims 1 and 2 will first be addressed.

The semiconductor apparatus of amended claim 1 includes a plurality of device elements formed on a surface of a semiconductor substrate. Each device element has a diffusion region. The semiconductor apparatus also includes a multi-layer wiring configuration electrically connecting at least two of the diffusion regions. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

As is well established, to anticipate a claim, a reference must teach every element of the claim. The cited reference *Hiraga* does not show a multi-layer wiring configuration electrically connecting at least two of the diffusion regions, where the multi-layer wiring configuration includes a plurality of wiring layers and a first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

FIG. 5 of *Hiraga* appears to illustrate a single wiring layer (bold lines in FIG. 5) used as a local interconnect to connect diffusion regions of a plurality of devices **30**. This wiring layer shows a wiring region in which wiring is provided in a horizontal direction and a region in which wiring is provided in a vertical direction. However, this single wiring layer is not part of a multi-layer wiring configuration. It is a single layer wiring configuration that is electrically connecting the diffusion regions of a plurality of devices **30**.

Nowhere in the specification is it indicated that the bold lines of FIG. 5 is a multi-layer wiring, as required by claim 1.

FIG. 3 of *Hiraga* does appear to illustrate a multi-layer VDD line. In this case, the VDD line (over the PMOS transistors in N-well **4**) is connected to line **5**. However, the VDD line does not include a first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction, as required by claim 1.

Accordingly, because the cited reference does not show all limitations of the claim 1, the rejection of claims 1 and 2 is traversed.

The rejection of Claims 7, 8, and 13 will now be addressed.

The semiconductor apparatus of amended claim 7 includes a plurality of functional circuit blocks, each functional circuit block including a plurality of device elements, a first wiring region and a second wiring region. Also included is a multi-layer wiring configuration electrically connecting predetermined ones of the device elements. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

To the extent this rejection relies on *Hiraga*, the arguments as set forth for claim 1 are incorporated herein. Namely, that while *Hiraga* shows a wiring layer connecting diffusion

regions of transistor devices, such a wiring layer is not a multi-layer wiring. Conversely, while *Hiraga* describes a multi-layer VDD line, such a line does not include a first one of a plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

Accordingly, because the cited reference does not show all limitations of claim 7, the rejection of claims 7, 8, and 13 is traversed.

Claims 1, 3, 4, 5, 7, 9, 10, 12, and 13 have been amended, not in response to the prior art, but to address objections and rejections based on 35 U.S.C. §112. The present claims 1-13 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Version With Markings to Show Changes Made

In the Specification.

Please replace the title beginning at Page 1, Line 1 with the following replacement title.

SEMICONDUCTOR APPARATUS **INCLUDING A MULTI-LAYER WIRING CONFIGURATION** AND MANUFACTURING METHOD THEREFOR

Please replace the paragraph beginning at Page 4, Line 22 with the following replacement paragraph.

It is noted that in FIG. 6, **[that]** first wiring layer **M1** is used for interconnect in the vertical direction within a conventional functional circuit block **600**. The second wiring layer **M2** is used for interconnect within the horizontal direction **[withing]** **within** the conventional function circuit block **600**. This allows a central region **610** to be used for block to block interconnections without the addition of a separate routing channel outside the parameters of the conventional function circuit block **600**.

Please insert the following paragraph at Page 3, line 1.

Referring now to FIG. 7, a conventional memory array is set forth in a block schematic diagram and given the general reference character 700. Conventional memory array includes capacitor over bit line (COB) memory cells MC connected by a bit line BL.

Please insert the following paragraph at Page 8, line 13.

FIG. 7 is a block schematic diagram of a conventional memory array.

Please replace the paragraph beginning at Page 9, Line 4 with the following

replacement paragraph.

As but one example, the material for the second and third wiring layers (**M2** and **M3**) can be aluminum. Aluminum can exhibit approximately a difference of two orders of magnitude lower sheet resistance than the high melting point metal. Although specific values can depend on film thickness, values of the sheet resistance of aluminum can be several tens of mΩ/□ and values of the sheet resistance of a high melting point metal can be several **[mΩ/□]** Ω/□.

In the Claims.

1. (Amended) A semiconductor apparatus, comprising:

a plurality of device elements formed on a surface of a semiconductor substrate, each device element having a diffusion region; and

a multi-layer wiring configuration electrically connecting at least two of the diffusion regions, the multi-layer wiring configuration containing a plurality of wiring layers, a first **[wiring layer]** **one** of the plurality of wiring layers being divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

3. (Amended) The semiconductor apparatus according to claim 2, wherein:

predetermined wiring in the first **[wiring layer]** **one of the plurality of wiring layers** is electrically connected to and disposed in parallel with wiring in a second **[wiring layer]** **one** of the plurality of wiring layers; and

the second **[wiring layer]** **one of the plurality of wiring layers** has a higher sheet resistance than the first **[wiring layer]** **one of the plurality of wiring layers**.

4. (Amended) The semiconductor apparatus according to claim 2, wherein the first **[wiring layer]** **one of the plurality of wiring layers** includes:

a first wiring trace in the second wiring region disposed in the second direction;

a second wiring trace in the second wiring region disposed in the second direction and separated from the first wiring trace in the first direction; and

a third wiring trace in the first wiring region disposed in the first direction and electrically connecting the first wiring trace and the second wiring trace.

5. (Amended) The semiconductor apparatus according to claim 2, further including:

the multi-layer wiring configuration includes a second one of the plurality f wiring layers;

a memory array having bit lines formed with **[a second wiring layer] bit line wiring layers of the same material as the second one of the plurality of wiring layers; and**

the second **[wiring layer] one of the plurality of wiring layers** has a higher sheet resistance than the first **[wiring layer] one of the plurality of wiring layers**.

7. (Amended) A semiconductor apparatus, comprising:

a plurality of functional circuit blocks, each functional circuit block including a plurality of device elements, a first wiring region and a second wiring region; and

a multi-layer wiring configuration containing a plurality of wiring layers for electrically connecting predetermined ones of the device elements, the multi-layer wiring configuration including a first **[wiring layer] one of the plurality of wiring layers** disposed in the first wiring region providing first wiring in a first direction and the first **[wiring layer] one of the plurality of wiring layers** disposed in the second wiring region providing second wiring in a second direction.

9. (Amended) The semiconductor apparatus according to claim 8, comprising:

a predetermined first **[wiring in] portion of** the first **[wiring layer] one of the plurality of wiring layers** is electrically connected to and disposed in parallel with wiring in a second **[wiring layer] one of the plurality of wiring layers** of the plurality of wiring layers; and

the second **[wiring layer] one of the plurality of wiring layers** has a higher sheet resistance than the first **[wiring layer] one of the plurality of wiring layers**.

10. (Amended) The semiconductor apparatus according to claim 9, wherein the second **[wiring layer]** **one of the plurality of wiring layers** has a higher melting point than the first **[wiring layer]** **one of the plurality of wiring layers**.

12. (Amended) The semiconductor apparatus of claim 8, further including:

the multi-layer wiring configuration includes a second one of the plurality of wiring layers;

a memory array having bit lines formed with **[a second wiring layer]** **bit line wiring layers of the same material as the second one of the plurality of wiring layers**; **and**

the second **[wiring layer]** **one of the plurality of wiring layers** has a higher sheet resistance than the first **[wiring layer]** **one of the plurality of wiring layers**.

13. (Amended) The semiconductor apparatus of claim 8, wherein the device elements are insulated gate field effect transistors (IGFETs), each IGFET having a source/drain diffusion region and the multi-layer wiring structure electrically connects a source/drain region of at least two IGFETs within a functional circuit block by using the first **[wiring layer]** **one of the plurality of wiring layers** in the first wiring region and the second wiring region.

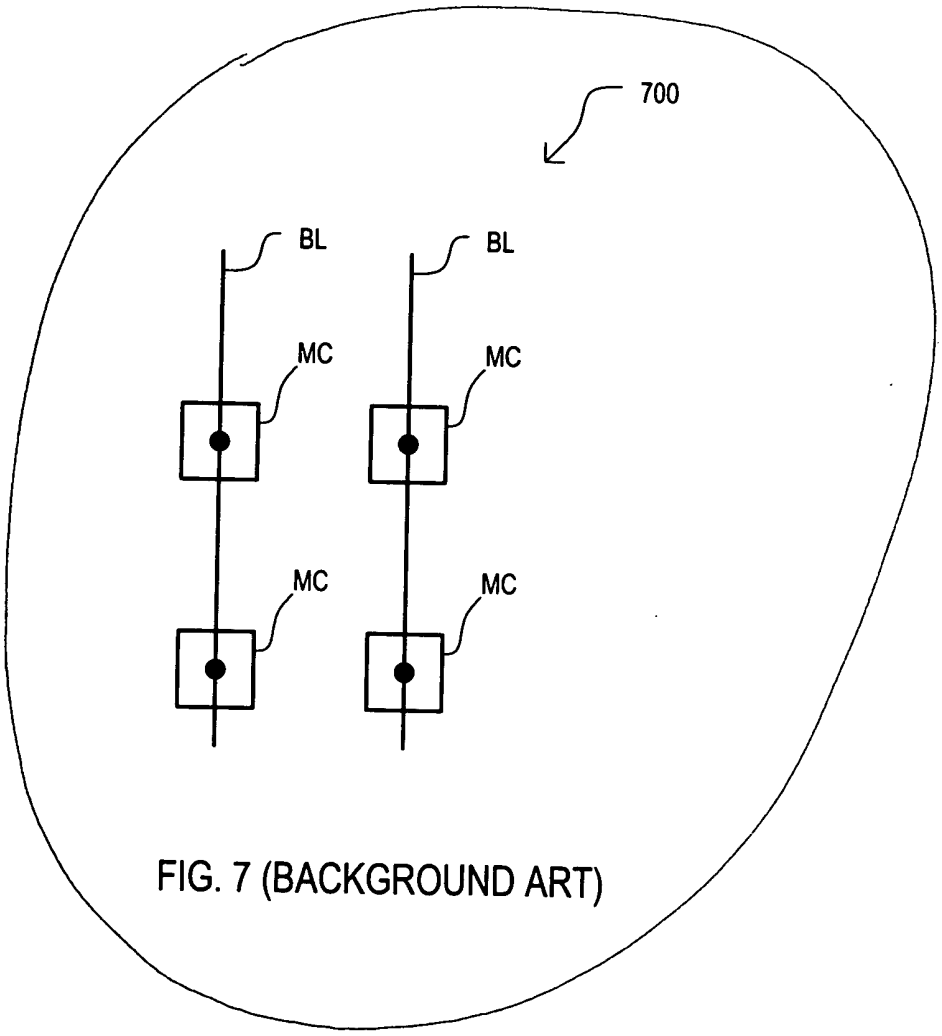

FIG. 7 (BACKGROUND ART)